Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-4, 6-18 and 20-26 are pending in the application, with claims 1 and 15 being the independent claims. Claims 1, 2, and 3-7 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding rejections and that they be withdrawn.

Rejections under 35 U.S.C. § 102

The Examiner has rejected claims 1, 3, 4, 8, and 9 under 35 under 35 U.S.C. § 102(b) as being allegedly unpatentable over U.S. Patent No. 5,003,462 to Blaner *et al.* (hereinafter, "Blaner"). Applicants respectfully traverse this rejection.

Independent claim 1, as amended herein, is directed to a method for processing data using a plurality of processing engines, the method comprising:

> processing first data associated with an older control record in a first processing engine;
>
> processing second data associated with a younger control record in a second processing engine;
>
> enabling a first interrupt indicator in the younger control record when the processing of the second data is completed; and
>
> moving the first interrupt indicator associated with the younger control record onto a second interrupt indicator associated with the older control record if processing of the second data completes before processing of the first data.

Blaner does not teach or suggest each and every one of the foregoing features of independent claim 1. For example, Blaner does not teach or suggest at least "processing first data...in a first processing engine" and "processing second data...in a second processing engine."

Blaner is directed to a system for precisely reporting interrupts in a pipelined instruction processor. *See* Blaner, col. 2, lines 40-46. Specifically, Blaner describes two different systems for reporting interrupts depending upon the associated type of interrupt issued. The systems include a dedicated hardware structure and a software based system. *See* Blaner, col. 2, lines 47-54. Virtual memory management interrupts (e.g. address translation lookaside buffer (TLB) miss interrupts) occur frequently and are therefore handled by the dedicated hardware structure disclosed in Blaner, which is able to process interrupts more rapidly than the software based system. All other remaining interrupts are handled using the software based system that, although slower, is further capable of precisely reporting the occurrence of an interrupt. *See* Blaner, col. 2, lines 47-62.

Regardless of how the precise reporting of an interrupt occurs in Blaner, all processing associated with a given interrupt is still done in a **single**, pipelined instruction processor. In contrast, however, claim 1 recites "processing first data...in a first processing engine" and "processing second data...in a second processing engine." Blaner does not parallel process first data in a first processing engine and second data in a second processing engine, let alone disclose even a first **and** second processing engine. All processing related to an interrupt occurs in the single, pipelined processor of Blaner. For this reason alone, Blaner cannot anticipate claim 1.

Furthermore, even if we assume, for the sake of argument, that Blaner discloses both first and second processing engines, Blaner still fails to teach or suggest "enabling a first interrupt indication in [a] younger control record when the processing of [a] second data is completed," as recited in claim 1. An interrupt indicator, as described in the present specification, "causes a core to **issue** an interrupt." *See* present specification, paragraph [0037]. (emphasis added). Blaner, as noted above, is directed to the reporting and handling of interrupts **after** they have been issued. Blaner mentions no equivalent structure, system or method, such as an "interrupt indicator," that causes a core to issue an interrupt when enabled. In summary, Blaner and the features of claim 1, fall on opposite sides of the interrupt process. Blaner is completely directed to tasks after an interrupt has issued (i.e., reporting and handling), while claim 1 is directed to tasks prior to the issuance of an interrupt.

Because Blaner does not teach each and every feature of claim 1, it cannot anticipate that claim. Dependent claims 3, 4, 8 and 9 are similarly not anticipated by Blaner for the same reasons as independent claim 1, from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 1, 3, 4, 8, and 9 under 35 U.S.C. § 102(b) be reconsidered and withdrawn.

Rejections under 35 U.S.C. § 103

Blaner in view of Pierson et al.

The Examiner has rejected claim 2 under 35 U.S.C § 103(a) as being allegedly unpatentable over Blaner in view of Pierson *et al.* (hereinafter, "Pierson"), "Context-

Agile Encryption for High Speed Communications Networks," Computer Communications Review, Association for Computing Machinery, Vol. 29, No. 1, January 1999, pp. 35-49. Pierson does not in anyway remedy the deficiencies of Blaner with respect to independent claim 1, as discussed above. Consequently, the combination of Blaner and Pierson cannot render independent claim 1 obvious. Claim 2 is similarly not rendered obvious by the combination of Blaner and Pierson for the same reasons as independent claim 1, from which it depends, and further in view of its own respective feature. Accordingly, Applicants respectfully request that the rejection of claim 2 under 35 U.S.C § 103(a) be reconsidered and withdrawn.

Blaner in view of Yamaura

The Examiner has rejected claims 6, 7, and 10-14 under 35 U.S.C § 103(a) as being allegedly unpatentable over Blaner in view of U.S. Patent No. 6,175,890 to Yamaura (hereinafter, "Yamaura"). Yamaura does not in anyway remedy the deficiencies of Blaner with respect to independent claim 1, as discussed above. Consequently, the combination of Blaner and Yamaura cannot render independent claim 1 obvious. Claims 6, 7, and 10-14 are similarly not rendered obvious by the combination of Blaner and Yamaura for the same reasons as independent claim 1, from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 6, 7, and 10-14 under 35 U.S.C § 103(a) be reconsidered and withdrawn.

Nakaya in view of Yamaura

The Examiner has rejected claims 1, 3, 4, and 6-14 under 35 U.S.C § 103(a) as being allegedly unpatentable over U.S. Patent No. 5,978,830 to Nakaya et al.

(hereinafter, "Nakaya") in view of Yamaura. For the reasons set forth below, Applicants respectfully traverse.

The combination of Nakaya and Yamaura does not teach or suggest each and every feature of claim 1, as amended herein. For example, Nakaya and Yamaura do not teach or suggest at least "moving [a] first interrupt indicator associated with [a] younger control record onto a second interrupt indicator associated with [an] older control record if processing of the second data completes before processing of the first data."

The Examiner, in the Response to Arguments section of the current Office Action, states that Nakaya teaches of both younger and older instructions that are comparable to the younger and older control records of claim 1, noted above. *See* present Office Action, page 3. Specifically, the Examiner refers to FIG. 7 of Nakaya and equates, for example, instructions U2 through U6, which are executed in parallel on separate processors P2-P6, as being younger instructions compared to instruction U1, executed on processor P1 (U1 being the older instruction). The Examiner then goes on to explain that "[a]n interrupt for any parallel computing part will not be issued until all of the multiple parallel computable parts (e.g. U2 through U6) are finished processing." *See* present Office Action, page 3.

Applicants wish to point out to the Examiner that the older instruction U1 can never finish **after** the parallel execution of younger instructions U2 through U6. Nakaya makes this specifically clear, stating that FIG. 7 is drawn "on the assumption that time flows from left to right," and that only the parallel computable parts, such as instructions U2-U6, have an "arbitrary execution order." *See* Nakaya, col. 12, lines 30-50. However, the serially executed instructions, such as U1, must complete before another instruction

executes — due to the fact the proceeding instructions depend on the result of U1's execution. The execution of younger instructions U2 through U6 only begins **after** the execution of instruction U1 has already completed, as shown in FIG. 7 of Nakaya. Consequently, Nakaya does not teach or suggest "moving a first interrupt associated with a younger control record onto a second interrupt indicator associated with an older control record if processing of the second data completes **before** processing of the first data," where the second data is younger then the first data, as recited in claim 1. (emphasis added). In fact, it would make no sense for Nakaya to teach this feature since the younger instructions U2-U6 always finish processing **after** the older instruction U1.

Furthermore, in Nakaya, the fact that "[a]n interrupt for any parallel computing part will not be issued until **all** of the multiple parallel computing parts (e.g. U2 through U6) are finished processing," as pointed out by the Examiner, is irrelevant. *See* present Office Action, page 3. (emphasis added). The features of claim 1 do not, in anyway contend delaying the issuance of an interrupt until **all** processing engines have completed their respective tasks. Rather, the invention of claim 1 results in delaying the issuance of an interrupt **only** if processing of the second, younger data completes before processing of the first, older data. Consequently, Nakaya not only fails to teach or suggest each and every feature of claim 1, but in fact teaches away from the presently claimed features.

Yamaura does not cure the deficiencies of Nakaya. Consequently, the combination of Nakaya and Yamaura cannot render independent claim 1 obvious. Claims 3, 4, and 6-14 are similarly not rendered obvious by the combination of Nakaya and Yamaura for the same reasons as independent claim 1, from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully

request that the rejection of claims 1, 3, 4, and 6-14 under 35 U.S.C § 103(a) be reconsidered and withdrawn.

Nakaya in view of Yamaura, further in view of Pierson

The Examiner has rejected claims 2, 15-18, and 20-26 under 35 U.S.C § 103(a) as being allegedly unpatentable over Nakaya in view of Yamaura, and further in view of Pierson. For the reasons set forth below, Applicants respectfully traverse.

Claim 2

Pierson does not in anyway remedy the deficiencies of Nakaya and Yamaura with respect to independent claim 1, as discussed above. Consequently, the combination of Nakaya and Yamaura cannot render independent claim 1 obvious. Claim 2 is similarly not rendered obvious by the combination of Nakaya, Yamaura, and Pierson for the same reasons as independent claim 1, from which it depends, and further in view of its own respective features. Accordingly, Applicants respectfully request that the rejection of claim 2 under 35 U.S.C § 103(a) be reconsidered and withdrawn.

Claims 15-18, and 20-26

Independent claim 15 is directed to a cryptography accelerator that includes the feature of "a history buffer containing information associated with the first and second control records including a first interrupt indicator associated with the first control record and a second interrupt indicator associated with the second control record, wherein the history buffer is configured to move the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record if processing of the first control record completes before processing of the second control record." As noted above in regard to claim 1, Nakaya does not teach or suggest moving

the first interrupt indicator associated with the first control record onto a second interrupt indicator associated with the second control record **if processing of the first control record completes before processing of the second control record**. Yamaura and Pierson do not cure the deficiencies of Nakaya. Consequently, the combination of Nakaya, Yamaura, and Pierson cannot render independent claim 15 obvious. Claims 16-18 and 20-26 are similarly not rendered obvious by the combination of Nakaya, Yamaura, and Pierson for the same reasons as independent claim 15, from which they depend, and further in view of their own respective features. Accordingly, Applicants respectfully request that the rejection of claims 15-18 and 20-26 under 35 U.S.C § 103(a) be reconsidered and withdrawn.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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